DETAILED ACTION

Claim Objections

1. Claims 33-35, 43, 105-107, 111, 125, 135-137, are objected to because of the following informalities: Appropriate correction is required.

In each of the claims above, the amorphous and polycrystalline materials that include the bracket with a comma "(,)" create vagueness. Thus, in this office action the examiner interprets the comma within the bracket to mean "and". For example, "(Ga,N)" is to mean "GaN" – Gallium Nitride .

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 30-31, 36-42, 46-49, 51-52, 78-80, 82, 102-103, 108-110, 114-123, 126-129, 132-140 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi (5,858,855) in view of Mackawa (6,066,547).

As to claim 30, Kobayashi discloses a method of bonding two structures together, the method comprising: depositing low temperature grown semiconductor bonding layers 2,12 (figs. 3B-3C) on first and second structures 1, 3 (figs. 3B-3C), placing the bonding layers 2, 12 (figs. 3B-3C) in contact with each other to form a combined structure (figs. 3B-3C); combining the two structures together creating an inherent pressure (figs. 3B-3C); and annealing the combined structure under conditions sufficient for the bonding layers to bond the first and second structures together (col. 2, lines 38-42). Note that bonding layers 2 and 12 are polycrystalline silicon.

However, Kobayashi does not explicitly teach that at least one of the bonding layers (polycrystalline silicon) begins with an amorphous (silicon) material; wherein the annealing step causes the amorphous material to crystallize at least a portion of the amorphous material to a polycrystalline material.

Mackawa discloses an analogous device (transistor) and method having a step of forming an amorphous silicon layer 14 (fig. 4) on a substrate 12 (fig. 4), wherein the amorphous silicon layer 14 undergoes an annealing process to crystallize the amorphous silicon to a polycrystalline silicon (col. 5,lines 25-50).

Therefore, as to claims 30-31, 47, 52,80, 102-103, 132-134, 138, it would have been obvious to one of ordinary skills in the art at the time the invention was made to construct the polycrystalline silicon layer 2 or 12 of Kobayashi with the amorphous silicon material that undergoes the annealing step to form a polycrystalline silicon material, as taught by Mackawa, for providing the same advantage and cost efficiency (col. 2, lines 3-5).

As to claims 36,118, the bonding layers 2, 12 are placed in contact with each other (figs. 3B-3C).

As to claims 37, 108, Mackawa teaches that the substrate 12 may be a quartz (col. 5, lines 40-42) for providing an enhanced mobility.

As to claim 38, the method includes making an electronic device (fig. 2).

As to claims 39, 109, the annealing step of Kobayashi permits the bonding of the combined structure (col. 2, lines 38-42).

As to claims 40-41,110, 139140, the bonding interface of Kobayashi meets the limitation of the claim.

As to claim 42, although Kobayashi in view of Mackawa does not teach a range of thickness for the bonding layers, it would have been obvious to one of ordinary skills in the art at the time the invention was made to construct a range of thickness for the bonding layers of Kobayashi as claimed, since it is a prima facie obvious to an artisan for optimization and experimentation to create a range of thickness for the bonding layers because applicants have not yet established any criticality for the range.

As to claims 46,114-115, a polycrystalline semiconductive layer 2 or 12 is deposited on one of the structures 1 or 3 (fig.3B-3C; col. 5, lines 25-45).

As to claims 48, 116the annealing occurs at most 800 Celsius. (col. 2, lines 1-40).

As to claim 49, Mackawa teaches the bonding layer 14 comprises a compound semiconductor (col. 5 ,lines 44-45).

As to claims 78-79, Mackawa teaches an insulator 16 (fig. 4).

As to claim 82, the bonding layers 2 or 12 are devoid of materials as claimed.

As to claim 117, Kobayashi teaches the doping of the bonding layers 2 or 12 with impurity. (col. 5, lines 25-35).

As to claims 120, 126, the bonding layers 2 or 12 have identical material.

As to claims 121, 127, the combined structure has an external pressure to combine the structures 1 and 3.

As to claims 122-123, 128-129, both polycrystalline silicon layers 2 or 12 of Kobayashi may start out as amorphous material as taught by Mackawa for the advantage as discussed in the above.

As to claim 123

Allowable Subject Matter

5. Claims 33-35, 43, 50, 53, 105-107, 111, 119, 124-125, 130-131, 135-137, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not disclose or fairly suggest either in singly or in combination a method having among others, the step of combining the bonding layers, wherein the bonding layers comprise at least one of amorphous (Ga,As) or (Ga,N) or (Ga,P) or (In,Ga,As) or (In,Ga,P) or

(In, Ga,As,P) and polycrystalline (Ga,As) or (Ga,N) or (Ga,P) or (In,Ga,As) or (In,Ga,P) or (In, Ga,As,P) and the annealing of the combined structure occurs at a temperature of between about 300°C and 500°C and for a time sufficient for the bonding layers to form a (Ga,As) or (Ga,N) or (Ga,P) or (In,Ga,As) or (In,Ga,P) or (In, Ga,As,P) material that is substantially entirely polycrystalline.

Response to Arguments

1. Applicant's arguments filed 06/08/2007 and subsequent Interviews with respect to the pending claims have been fully considered and are persuasive. The final Office Action sent on and the premature advisory action have been withdrawn.

2. Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to (Vikki) Hoa B. Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Thursday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 571-273-8300. Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

/(Vikki) Hoa B Trinh/

Examiner, Art Unit 2814

/Howard Weiss/
Primary Examiner, Art Unit 2814